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13. ABSTRACT (Maximum 200 words) "This report was developed under SBIR Contract" for topic, "Army 00-019." This report describes the design and development of a high-speed, high-resolution wavefront sensing and control system. The system will couple high-resolution analog liquid crystal spatial light modulators with an innovative subtractive imaging sensor. The resulting system will achieve vast improvements in resolution, size, weight and cost over currently available systems.				
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Phase I Final Report

A High-Resolution Wave-front Sensing and Control System

ARMY Contract #DAAD19-01-C-0009

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1	INTRODUCTION TO PHASE I RESEARCH.....	4
1.1	THE NEED FOR WAVE-FRONT SENSING & CORRECTION.....	4
1.2	PHASE I TECHNICAL TASKS.....	5
1.3	STRUCTURE OF THE PHASE I FINAL REPORT.....	6
2	TECHNICAL BACKGROUND.....	6
2.1	FABRICATION OF LC SPATIAL LIGHT MODULATORS.....	6
2.2	LIQUID CRYSTAL MODULATORS	7
3	PHASE I TECHNICAL EFFORT	9
3.1	THE WAVE-FRONT SENSING SYSTEM	9
3.1.1	<i>System Components</i>	9
3.1.1.1	DALSA Camera.....	10
3.1.1.2	National Instruments Data I/O Board	10
3.1.1.3	EPIX Frame Grabber	10
3.1.1.4	BNS 512x512 Prototype Driver Board.....	10
3.1.1.5	BNS 512x512 Liquid Crystal Spatial Light Modulator	13
3.2	THE SUBTRACTIVE IMAGER.....	14
4	PHASE I RESULTS	15
4.1	SLM MODULATION CHARACTERISTICS	15
4.2	WAVESENSE SOFTWARE	17
4.2.1	<i>DALSA Camera Image</i>	19
4.2.2	<i>Display Options</i>	19
4.2.2.1	Zoom.....	19
4.2.2.2	DC.....	19
4.2.3	<i>Calculated Values</i>	19
4.2.3.1	Peak	19
4.2.3.2	Centroid	20
4.2.3.3	Fixed Location	20
4.2.3.4	1st Moment	20
4.2.3.5	Strehl Ratio	20
4.2.3.6	Strehl Radius.....	20
4.2.3.7	Noise Floor	21
4.2.3.8	Normalize	21
4.2.4	<i>Phase States</i>	21
4.2.5	<i>Phase Image Generation Options</i>	21
4.2.5.1	Circle Option	22
4.2.5.2	SLM=DALSA Option.....	22
4.2.5.3	LUT File	22
4.2.5.4	Threshold Option	23
4.2.5.5	Alignment Mode Option.....	23
4.3	WAVE-FRONT SENSOR SPEED.....	24
4.4	SUBTRACTIVE IMAGER TEST RESULTS	26
5	CONCLUSIONS AND RECOMMENDATIONS.....	28
5.1	SPEED IMPROVEMENTS.....	28
5.1.1	<i>Electronic Speed Improvements</i>	28
5.1.1.1	Use the PCI Bus.....	29
5.1.1.2	Pre-Store all Images.....	29
5.1.1.3	Direct feed through an External Port	29
5.1.1.4	Calculated Processing on SLM driver board.	29
5.1.2	<i>SLM Speed Improvements</i>	29

5.1.2.1	Use High Voltage VLSI Backplanes	29
5.1.2.2	Implement Cover Glass Flipping	30
5.1.2.3	Dual-Frequency LC Materials	31
5.2	SLM FLATNESS IMPROVEMENTS.....	33

1 Introduction to Phase I Research

This document is the final report for the Phase I Small Business Innovative Research (SBIR) contract #DAAD19-01-C-0009, awarded to Boulder Nonlinear Systems, Inc., in response to DOD SBIR solicitation topic A00-024, "Wave-front Control and Sensing System based on a Opto-Silicon Integrated Phase-Contrast Technique." The SBIR contract was awarded through the U.S. Army and administered through the U.S. Army Research Office. The optical architecture and algorithms used in this system is based on the original work at the Army Research Laboratory (ARL).¹ The research presented subsequently is the result of a collaborative effort between Boulder Nonlinear Systems (BNS), Dr. Eric Justh, Dr. Ralph Etienne-Cummings and his group at Johns-Hopkins University (JHU), and the Intelligent Optics Laboratory at ARL. The purpose of the Phase I research was the development of a novel, liquid crystal based, analog phase wave-front sensing and compensation system. Phase I research concentrated on development and demonstration of the major components of the wave-front sensor, namely the Liquid Crystal Spatial Light Modulator (SLM) and the Subtractive Imager². The completed prototype SLM system was sent to ARL and evaluated by researchers there.

1.1 The Need for Wave-front Sensing & Correction

The phase-contrast wave-front sensing system described in this report addresses the Army's need for direct, high-resolution sensing and correction of wave-front phase. The architecture is particularly well suited for use in laser communications and other applications where the light source is monochromatic and coherent. Direct measurements of phase by the wave-front sensor will eventually feedback to a wave-front corrector in a stable control loop.

Figure 1 shows the complete phase-contrast wave-front sensing and correcting system as presented in the Phase I proposal. The input light is first corrected by the phase correcting spatial light modulator (SLM). The light is then focused down to the Fourier plane, where the DC component is phase shifted between two states, a $\pi/2$ shift and a $-\pi/2$ shift, by the Fourier Filter SLM. The Fourier Domain Camera constantly tracks the location of the DC component, and that information is sent back to the modulating Fourier Filter SLM. The two shifted images are then imaged onto the wave-front sensor

¹ Carhart, G. W.; Vorontsov, M. A.; Justh, E. W., "Optoelectronic Zernike filter for high-resolution wave-front analysis using phase-only liquid crystal spatial light modulator", Proc. of the SPIE, 4124, pp. 138-147, 2000.

² Gruev, V. and Etienne-Cummings, R., "A Pipe-Lined Differencing Imager," accepted for IEEE ISCAS'02, Tempe, AZ, May 2002.

camera, which subtracts the two images from each other, resulting in an image whose intensity is proportional to the phase measured. The resulting measurement is then fed back to modify the corrections applied by the phase correcting SLM. Phase I research concentrated on prototyping the advanced phase contrast sensor(within the dashed line in Figure 1) and the Subtractive Imager chip, to be used eventually as the wave-front sensor camera.

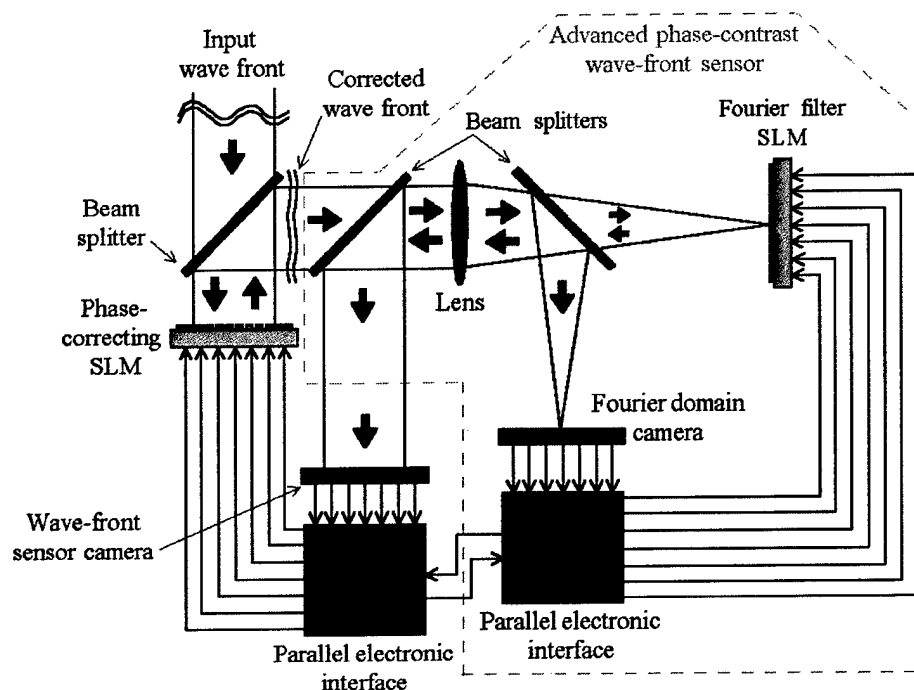


Figure 1. A High-Resolution Phase Contrast Wave-front Sensor & Correction System.

1.2 Phase I Technical Tasks

In Phase I research, the overall goal was to prototype the phase contrast wave-front sensor, evaluate its behavior, and determine the feasibility of developing the complete closed-loop system. Phase I technical task performance was key to determining the feasibility of the complete system. These tasks, as defined in the original Phase I proposal, are:

- Fabricate 512x512 NLC-SLM
- Characterize 512x512 NLC-SLM modulation characteristics
- Acquire a 512x512 off-the-shelf camera and frame grabber,
- Determine electronic processing requirement on wave-front sensor,
- Write software,
- Evaluate wave-front sensor subsystem,
- Electrical test of 128x128 Subtractive Imager chip,

- Determine electronic processing requirements for the subtractive imager,
- Redesign 128x128 Subtractive Imager,
- Preliminary design of 128x128 interface electronics,
- Write Final Report.

1.3 Structure of the Phase I Final Report

The final report is divided into four sections:

Section 2 contains background information and basic physical principles that produced the wave-sensing system. A discussion of LC-SLM fabrication and modulation principles is presented.

Section 3 describes the Phase I technical effort. The system construction and operation is described fully. In addition, the basic design of the subtractive imager is presented.

Section 4 contains all the Phase I work performed. Operation of the Phase I hardware is described, as well as a full description of the software interface and algorithms used.

Section 5 summarizes the Phase I research. Based on the knowledge gained in Phase I, BNS provides recommendations for further development in Phase II.

2 Technical Background

2.1 Fabrication of LC Spatial Light Modulators

A typical Liquid Crystal (LC) SLM is manufactured by first designing the silicon SLM backplane chip. This entails learning all of the details of the specific foundry process as no two processes are identical. The design must also be simulated in great depth due to the high cost associated with silicon foundry runs. These costs are mainly in the production of the very high-resolution masks required for each layer of the chip.

Once BNS has received the silicon chips they are placed into a carrier such as a ceramic Pin Grid Array (PGA). The PGA acts as a mechanical and electrical interface to the silicon chip. The chip must be wire bonded to the PGA package, hence connecting the chip electrically to the pins on the back of the PGA carrier (see Figure 2).

The next step is to add alignment layers to the silicon chip and to an Indium Tin Oxide (ITO) coated cover-glass. The ITO coating on the cover-glass is a thin transparent metal coating that provides an electrode for generating the desired field across the LC cell. The alignment layers provide a force to align all of the liquid crystal molecules into the same orientation. Without the alignment layers the LC alignment would be random and hence provide no useful optical modulation. The cover-glass is then bonded to the silicon chip using adhesive and small micro-balls or spacers. These spacers provide a uniform gap across the entire surface of the chip that is only a couple of microns thick.

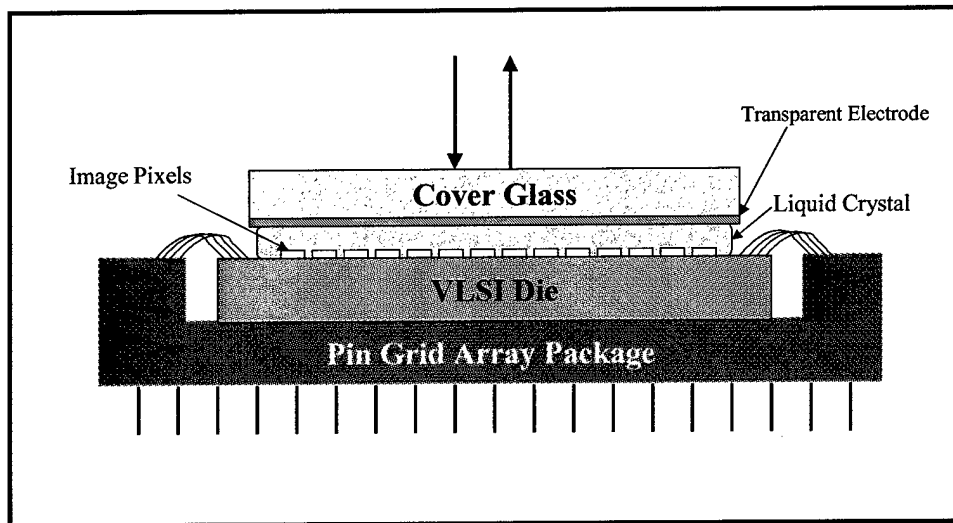


Figure 2. Drawing of an assembled SLM in cross-section.

This assembled unit is then placed in a vacuum chamber. While under vacuum, the chip is heated and the uniform gap is then filled with the desired LC material. After the vacuum is removed and the device cooled to room temperature, an electrode wire is attached to connect the ITO layer on the cover-glass to a pin on the PGA carrier. At this point, the SLM is complete and ready for testing.

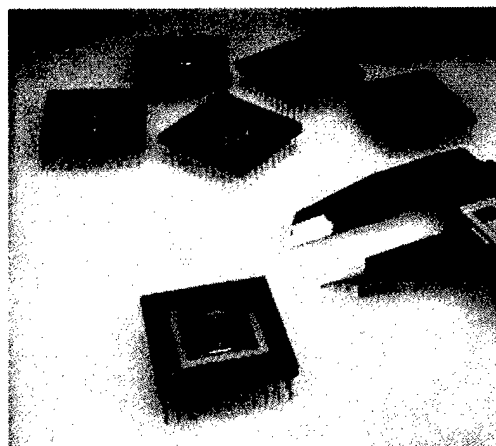


Figure 3. Photograph of several multi-level SLMs.

2.2 Liquid Crystal Modulators

Liquid crystal is a birefringent material. As polarized light enters the LC layer, the material performs two basic functions, wave division and retardation. That is, the liquid crystal divides a single wave, which is linearly polarized, into two orthogonally polarized waves and induces a time delay between these waves. This time delay occurs because

the crystalline structure of the LC material is such that the index of refraction is not the same in all directions. If an analyzing polarizer is placed after the device, the two waves are forced to interfere. If the two waves are in phase, light is strongly transmitted. If the two waves are out of phase, destructive interference occurs and the light is dissipated at the polarizer. Whether the two waves are in phase depends primarily on three things: (1) the birefringence of the LC material (or the difference in the index of refraction of the two paths), (2) the thickness of the LC layer, and (3) the wavelength of the input light. As an electric field is applied to a nematic LC layer, there is a corresponding reduction in the birefringence of the LC material. The birefringence change induces a phase-only modulation of the input light.

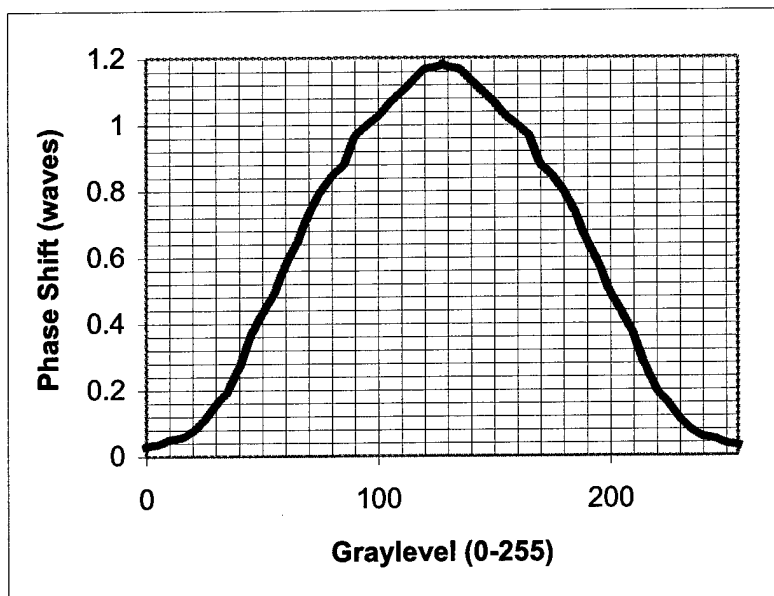


Figure 4. Typical response curve of a nematic LC-SLM.

Figure 4 shows the typical response curve for a nematic LC-SLM. The SLM pixels can be programmed to 256 (8-bit) gray-levels or voltage steps between 0–5 V. The cover glass electrode is set to the mid-range of 2.5 V. The symmetric nature of the curve above is due to the fact that nematic LC responds only to the strength of the electric field, not the sign. For example, a gray-level of 51 would result in a voltage of $((51/256)*5V)$ or 1.0 V. The difference between the pixel voltage (1.0V) and the cover glass (2.5V) results in a -1.5V field. Likewise, a gray-level of 205 results in a pixel voltage of 4.0 V, and a field of +1.5V. Since the LC only responds to the field strength, the same phase response is seen for grayscale 51 and 205. Therefore, despite 8-bits of pixel voltage addressing, only 7-bits of phase response is achieved.

3 Phase I Technical Effort

Two major accomplishments occurred over the course of the Phase I effort. First, BNS, in collaboration with Dr. Justh, developed a prototype wave-front sensing system for tracking the DC component in the Fourier plane, and relaying that information back to the Fourier filter SLM. Second, Dr. Etienne-Cummings and his group at Johns Hopkins University fabricated a prototype subtractive imaging chip.

3.1 The Wave-front Sensing System

Figure 5 is a diagram showing the prototype wave-front sensor developed by BNS in Phase I. BNS purchased an off-the-shelf PC as the host for the system. Imagery of the Fourier Plane is captured using a high-speed camera, and is transferred to the PC via a frame grabber card. Software in the PC analyzes the captured Fourier Plane image, and determines the location of the DC component. The software then determines the appropriate modulation image and transfers that image to the LC-SLM via the data I/O card in the PC and the 512x512 Drive electronics.

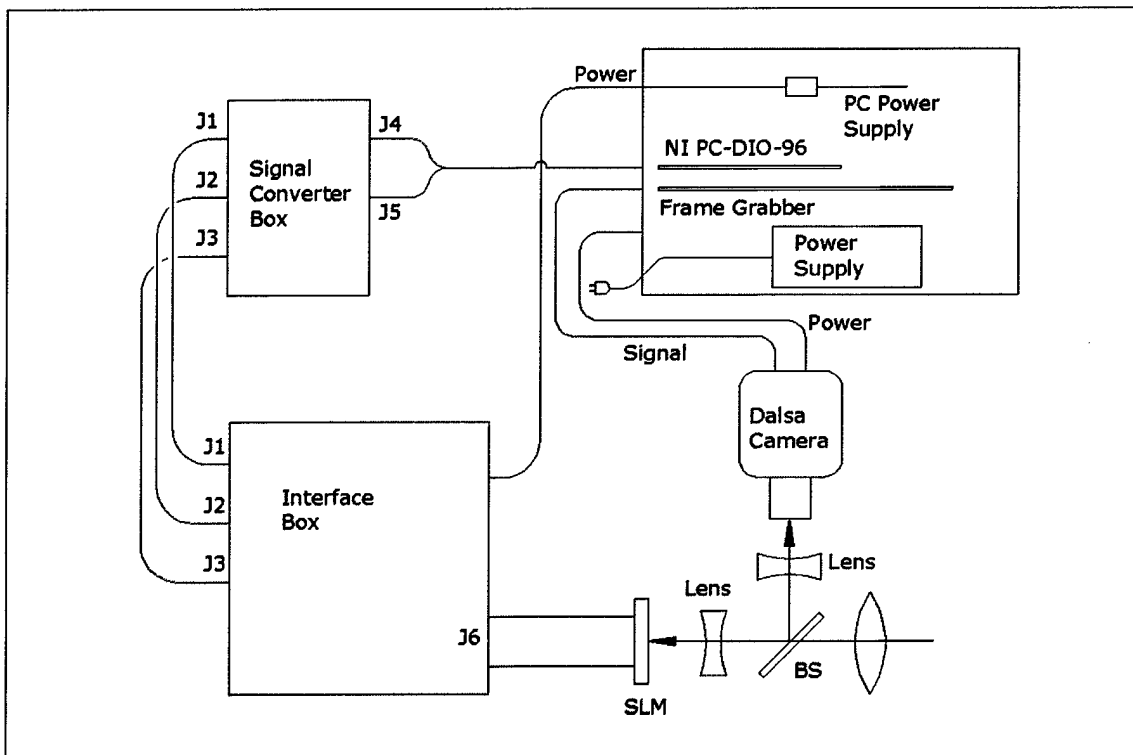


Figure 5. The Prototype Wave-front Sensor developed by BNS.

3.1.1 System Components

Most of the components used in the wave-front sensing system were off-the-shelf components, with the exception of the LC-SLM and its drive electronics, which were developed by Boulder Nonlinear Systems.

3.1.1.1 DALSA Camera

The area scan CCD camera used in the system was manufactured by DALSA in Ontario, Canada. The model used for the system is part number #CA-D6-0512W (\$5,900). This camera is high-speed (262 frames per second), and high resolution (532x516) with 100% fill factor. The pixels are square, and are pitched on 10 μ m centers. There are two cables that plug into the back of the camera, a data cable which connects with the EPIX frame grabber board, and a power cable, which connects to an accessory power supply, bolted inside the PC for convenience.

3.1.1.2 National Instruments Data I/O Board

The data I/O board used was the PCI-DIO-96 #777387-01 (\$295), manufactured by National Instruments of Austin, Texas. The PCI-DIO-96 has 96 TTL-level digital lines that can be configured as 8-bit output or input ports. The BNS 512x512 Prototype driver board was originally designed for the #PC-DIO-96 (now discontinued), which used an ISA slot for data transfer instead of the PCI slot used by the #PCI-DIO-96. Unfortunately, when converting to the PCI version of the board, National Instruments removed an onboard-timer that was being used by the original BNS design. To fix this problem, BNS had to design a hardware fix that automatically DC-balanced the LC-SLM, instead of relying on the onboard-timer/software balancing previously used.

A cable was also purchased #182762-01(\$65) to interface the Data I/O card with the driver board.

The National Instruments #PCI-DIO-96 came with a Windows-based device driver and a software dynamic-link library to drive their board. At system integration, however, BNS discovered this library was too slow, and therefore re-wrote the device driver.

3.1.1.3 EPIX Frame Grabber

The frame grabber used in the system was part number #PIXCI-D32-CA-D^A-0512W (\$1295) and was manufactured by EPIX, Inc. in Buffalo Grove, IL. This frame grabber line is specifically designed to interface to DALSA fast framing digital cameras. The frame grabber can support a sequential operating speed of 180 Hz for a 512x512 image.

A custom cable, part number #CBL-D32-CA-D6-0512W-2M (\$395) was also purchased to interface the Frame Grabber to the DALSA camera.

The EPIX frame grabber comes with XCLIB (\$495), a Windows NT software library for interfacing to the Frame Grabber, and a device driver, XCAP.

3.1.1.4 BNS 512x512 Prototype Driver Board

A driver board developed by Boulder Nonlinear Systems drives the LC-SLM. The driver board system, as shown in Figure 1, consists five separate boards; the data I/O board, the signal converter board, the interface board, the op-amp board and the SLM mount board. The data I/O board is the National Instruments board discussed in section 3.1.1.2. This board provides the parallel I/O interface needed to operate the SLM

system. It plugs into an ISA bus slot in the PC and converts 16-bit data transfers across the ISA bus into 64-bit data transfers to the SLM system. The signal converter board simply routes the appropriate signals from the data I/O board to the Interface board and converts them from TTL-levels to RS-422 levels. 512x512 image data is loaded through the data I/O board and signal converter board to the Interface board. The SLMs interface board, which is the large printed circuit board shown in Figure 6, is designed for high-speed data transfers (64 bits at 33 MHz), therefore it uses RS-422 differential drivers and receivers. The Interface board contains memory for two images, the true image and the inverse image. When operating, the hardware quickly toggles between these two images to provide DC balancing for the LC-SLM. The Interface board continuously pumps the two images to the LC-SLM at a load rate of 246 μ sec per image. Image data (eight bits digital) is first converted to an analog signal, and then amplified to the right levels for the LC-SLM by the op-amp board.

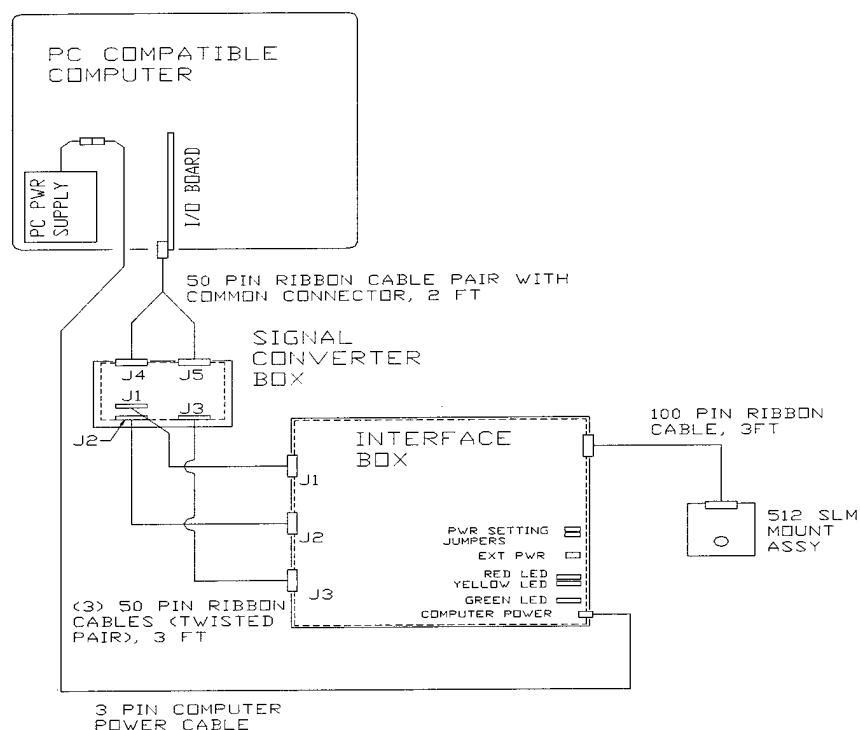


Figure 6 The 512x512 driver board system.

During power up there are three LEDs that are used to monitor the power. These LEDs can be viewed through the slot on the front left side of the Interface Board. The green LED will light up after the computer is turned on if there is the required 4A @ 5VDC available from the computer power supply. The yellow and red LEDs will turn on when there is the required 3A @ 5VDC and 2A @ 12VDC from either the computer power supply or an external supply.

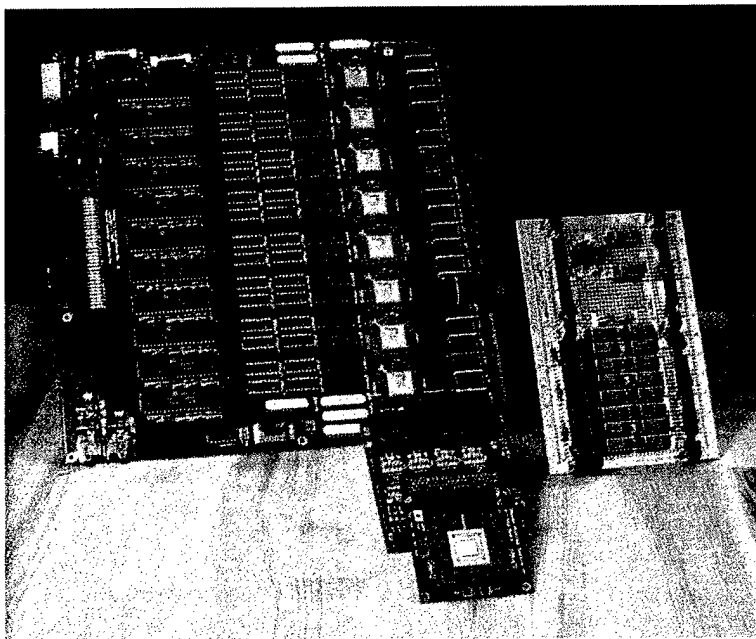


Figure 7. Components of the 512x512 multi-level SLM system.

To illustrate the basic drive scheme used in the SLM system, a block diagram is shown in Figure 8. The driver board receives 64 bits of data per clock strobe across a dedicated bus. This data is stored in a dual port memory. This dual port memory is deep enough to store two full frames of data. Therefore, the dual ports continually write the SLM from one port as new data is asynchronously loaded using the other port. With this dual port memory scheme, continuous operation at 2,000 frames per second is possible.

Four bits per pixel are stored in memory, but the data stored by the driver board is converted to analog levels by a high-speed, 8-bit digital-to-analog converter (DAC). A look-up table (stored in PROM's) converts the stored 4-bit digital data into 8-bit voltages. This allows the user to compensate for the nonlinear response of the LC modulator without requiring the storage and transfer of more data bits to drive the DACs. With a 4-to-8-bit look-up table (LUT), only four data bits per pixel are sent to the interface board, but the interface controls the optical modulator with eight bits of resolution. The LUT scheme also simplifies DC balancing since one of the remaining bits is used to invert the analog data during the load cycle. This bit is automatically controlled by the SLM interface board.

Our current DAC design settles to the appropriate voltage level in approximately 22 ns. This conversion rate allows data to be clocked into the SLM at 33 MHz. In the driver board design, 32 analog lines are loaded per clock cycle. Therefore the effective driver board to SLM data rate is 8.45 Gb/s. At this data rate, a full frame is loaded in 246 μ s (or 4069 fps).

subsequently designed with first-phase WHSC funding and test chips were fabricated during the final funding period. Because the program was limited, only prototype chips were fabricated and tested.

Our objective was to design a 512x512 VLSI chip that demonstrates 4kHz operation. In parallel with the VLSI design and fabrication, BNS developed a custom prototype board for driving this chip. The integrated system successfully demonstrated the desired information throughput requirements, which was the goal of first-phase. This was accomplished using an off-the-shelf National Instruments interface board that does not support fast loading of new data.

The SLM receives the 32 analog data lines, a clock signal, and 2 digital control bits (reset and row enable) from the driver board. All the analog signals are sent to the SLM mount board using current-mode drivers to prevent noise coupling. Current-to-voltage converters, on one of the two mount boards, drive the SLM chip. Because of the high-density design (15-micron pixel pitch), these analog drive signals must not exceed 5 volts. For the digital signals, an emitter coupled logic (ECL) interface is used. These digital signals not only require precise timing, but the SLM chip requires a clock that is two times faster than the data rate (i.e. 66 MHz clock for 33 MHz operation).

At the start of a frame, the reset signal initializes the on-chip timing circuit. This timing and control circuit uses the input clock to sequentially route the 32 analog signals to 16 different columns within the array (i.e. 32 signals times 16 columns equals 512 pixels per row). In turn, each row is activated by shifting a single bit (row enable) down a 1x512 shift register. This combination of routing and shifting allows analog data to be stored at each pixel within the 512x512 array. Each pixel is a small sample and hold circuit. It, therefore, captures the voltage level on a particular data line and holds it until the next frame cycle. Each pixel stores the analog data in a capacitor that consists of two metal pads separated by a thin dielectric layer.

3.2 The Subtractive Imager

During Phase I work, Dr. Ralph Etienne-Cummings and his student, Viktor Gruev, developed a 189x182 subtractive imager chip. The device automatically detects and computes temporal differences between two images. In-pixel storage elements for previous and current frames are provided. This device was fabricated using an AMI 0.5 μ m process. The imager pixels are 25 μ m x 25 μ m, with a fill factor of 30%. An efficient pipeline architecture for difference readout is implemented, allowing 8 bit precision of the difference imager. The integration time and the inter frame delay can be easily varied, without sacrificing the accuracy of measured difference.

The subtractive imager consists of four main components: a 189 x 182 photo pixel array, vertical and horizontal scanning registers, a control timing unit and a correlated double sampling unit. Each pixel has two outputs; a current frame output and a previous frame output. The reset offset mismatches between the two pixel outputs are

corrected in the correlated double sampling circuit. The difference between the two corrected values is then computed and provided outside the chip. The control timing unit synchronizes the timing between all scanning registers and employs an efficient pipeline mechanism for computing the difference between the two consecutive images. This unit also controls the integration time of the two frames, the time between consecutive frames, the sample/hold and subtraction timing of the correlated double timing sampling circuit. Different readout techniques can be executed by changing bit patterns in the scanning registers and reprogramming the control timing unit.

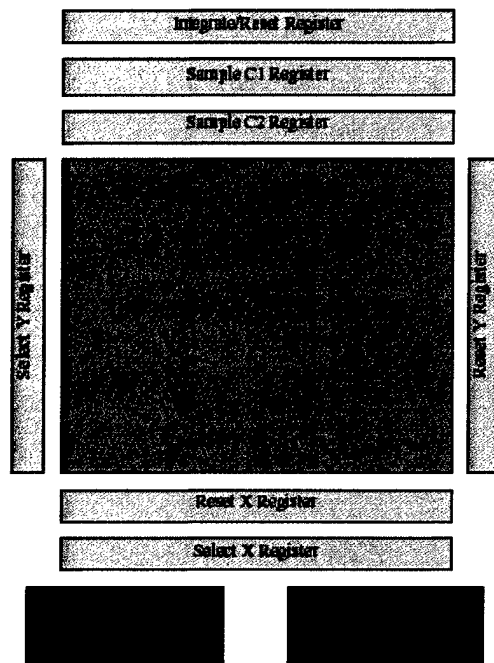


Figure 9. A block diagram of the subtractive imaging chip.

The TDI can be programmed to operate in two different modes, snapshot mode and pipeline mode. In snapshot mode, the first images is captured and stored, then the second image is captured and stored, and finally the entire difference between the two stored values is evaluated. In pipeline mode, the difference is calculated on a piece by piece basis as soon as the data on the second image is available.

4 Phase I Results

4.1 SLM Modulation Characteristics

Researchers at ARL measured the modulation depth produced by the device when applying different gray-levels to the pixels. The measurement was made by averaging the phase of a 1x96 area in the center of the array. The result of this measurement is

shown in Figure 10. Note that multiple gray levels produce the same phase. This is a result of the fact that the prototype hardware only supports 4 bits of image data storage, allowing only 16 phase levels. An on-board hardware look-up table converts the 4-bit data value into an 8-bit voltage, allowing more accuracy or linearization in the phase levels produced.

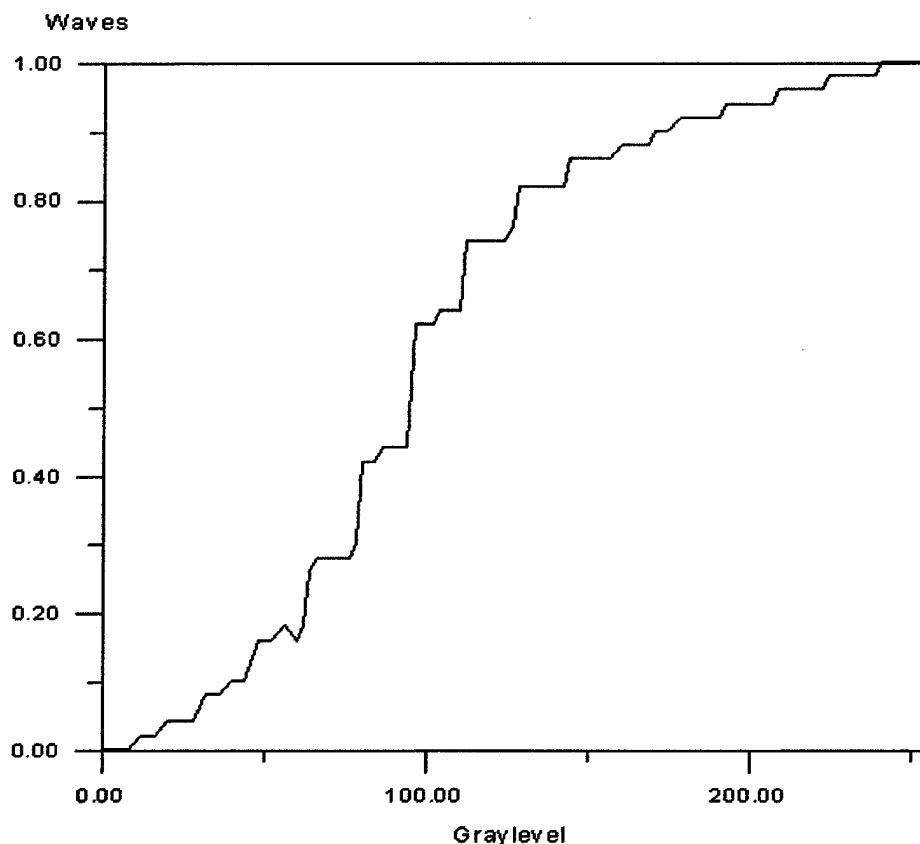


Figure 10. Phase Shift vs. gray level. The measurements were taken at 633nm.

A qualitative measurement of the phase contrast mechanism was also made. Figure 11 shows the output captured at the image plane camera. Multiple images are shown, resulting from phase shifting circles of varying radius. This is not the difference image, but is instead the image that results from shifting the DC component $+\pi/2$. The measurement shows a very good agreement between the original phase reference and the intensity measurement at the image plane when the radius of the shifting spot is sufficiently large.

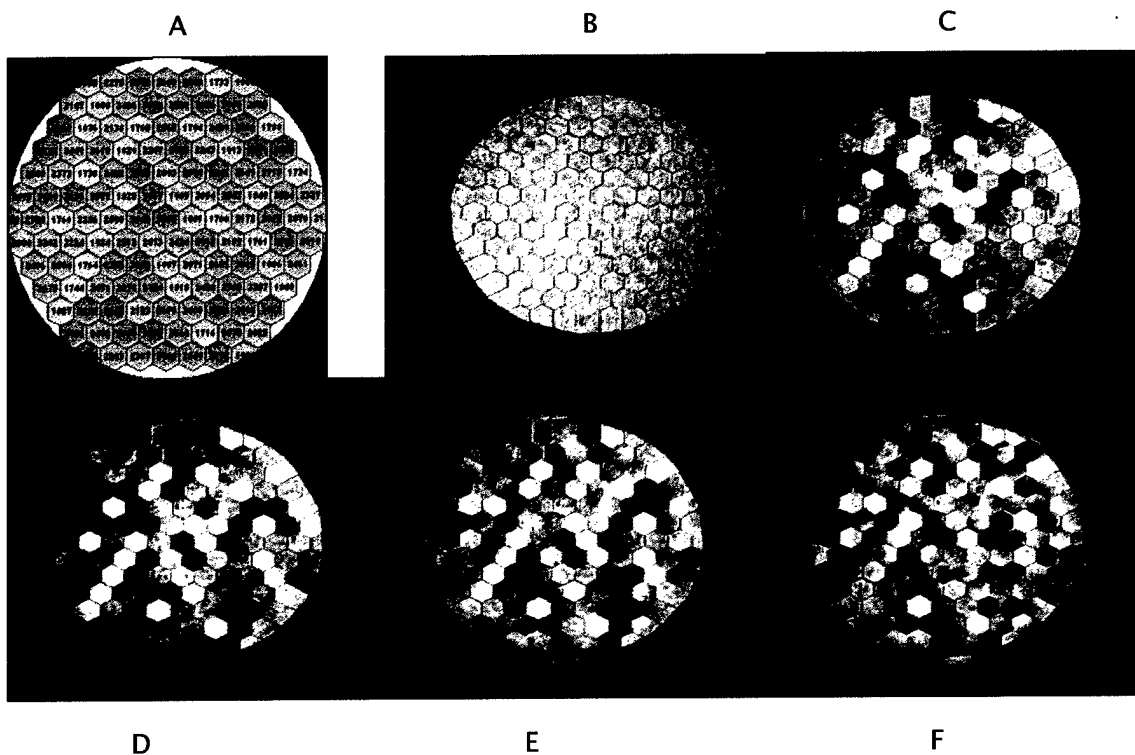


Figure 11. The image plane, captured as the phase shifting spot increases in radius from 0 (B), to 2(C),3(D) 4(E), and 5(F). The reference phase image is shown in (A).

4.2 WaveSense Software

The software created under this program is called *BNSWaveSense*. The application is a 32-bit Windows application, created with Microsoft Visual C++ 6.0. A shortcut to the executable program is on the system desktop.

The *BNSWaveSense* software communicates with two external devices, the EPIX frame Grabber and the National Instruments Board. Both of these devices require the installation of a device driver through the "Add New Hardware" section of the Windows Control Panel. The Epix Driver can be found in the directory *c:\xcap\drivers*. The National Instruments driver was developed by BNS, and can be found in the directory *C:\Program Files\Microsoft Visual Studio\MyProjects\BNS512\sys\i386\checked\bns512.sys*.

Figure 12 shows the user screen for *BNSWaveSense*. The screen is segmented into six distinct areas, each of which is discussed in more detail in the following sections.

The application is based on a basic state machine, as shown in Figure 13. Imagery of the Fourier plane is grabbed by the EPIX frame grabber and loaded into memory. The image is processed to determine the peak power point, the centroid, the Strehl ratio etc. From there, the SLM is modulated through a series of modulation states (normally $+\pi/2$

and $-\pi/2$ phase shifting circles). The entire process is then repeated until the user selects the Exit button.

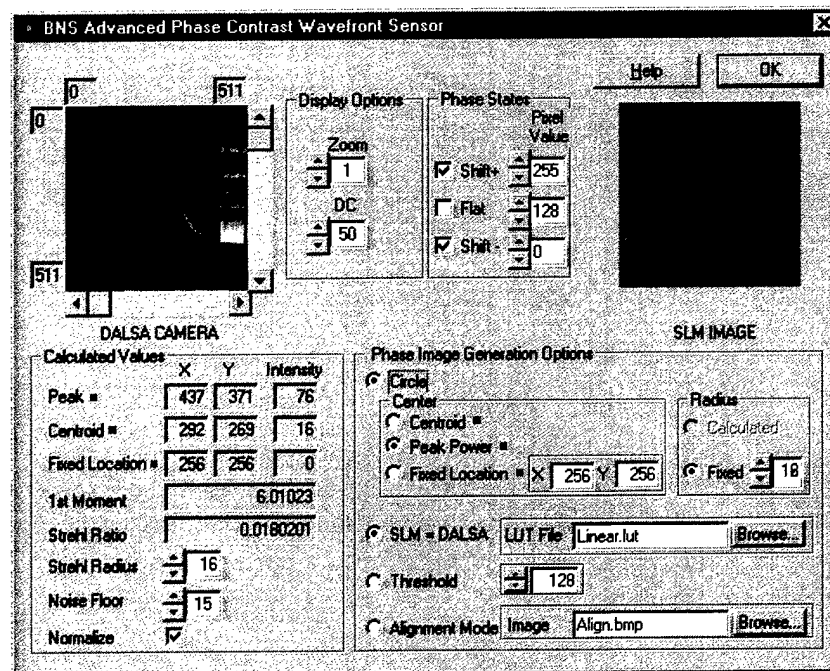


Figure 12. The *BNSWaveSense* User Screen.

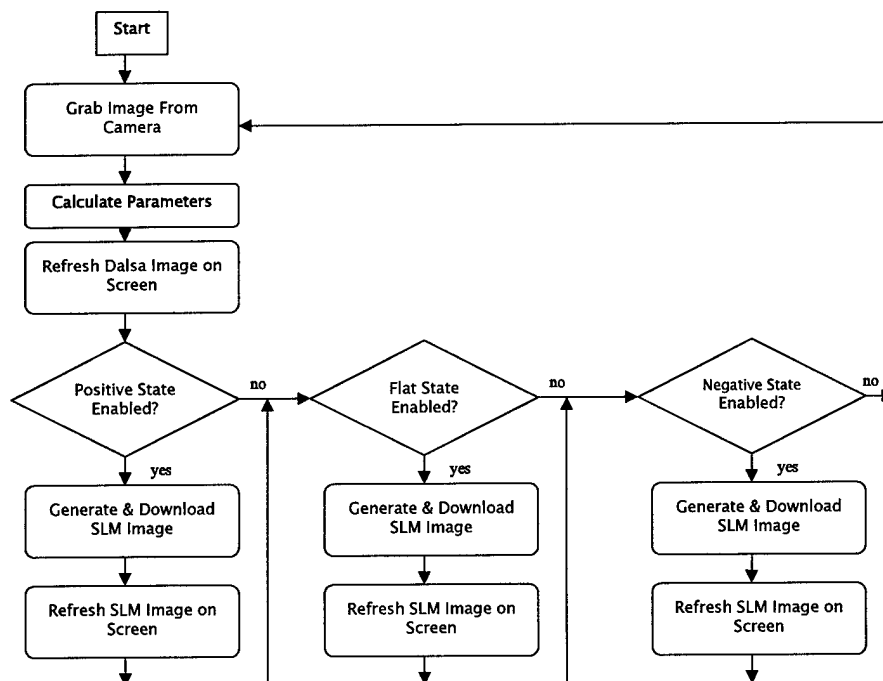


Figure 13. The *BNSWaveSense* state machine.

In the course of running the software, the user selects various parameters that determine the operation of the software. These parameters are automatically saved when the user exits the program, and reinstated when the program is re-executed.

4.2.1 DALSA Camera Image

The image captured from the DALSA camera is displayed in the upper left corner of the screen in a region defined by 128x128 pixels. The camera image pixel coordinates range from 0-511 in both the x and y dimensions. Parts of the camera image can be viewed in more detail by using the ZOOM feature and then using the horizontal and vertical scroll bars (below and right of the camera image) to move to the region of interest. The coordinates of the currently displayed x-axis are shown above the camera image, and the coordinates of the currently displayed y-axis are shown to the left of the camera image. The Display Option "DC" is added to the value of every pixel before it is displayed. The calculated peak power pixel is colored red, but is only visible when zoomed in. Likewise, the calculated centroid is colored blue and the fixed center pixel (defined in Phase Generation Options) is colored green.

4.2.2 Display Options

4.2.2.1 Zoom

The zoom factor determines how much of the DALSA camera image and the SLM image are displayed on the screen. Both of these images are displayed in a 128x128 pixel window. For a Zoom factor setting of n , a region of size $(512/n) \times (512/n)$ pixels is displayed on the screen. Valid values for Zoom factor are 1, 2, 4, 8, 16, 32, 64, and 128.

4.2.2.2 DC

The value of DC only affects how the DALSA image looks on the display. Valid values range from -255 to +255. The value of DC is added to every pixel value of the camera image before it is displayed. This feature is particularly useful at low-light levels, and assists the user in detecting intensity differences between low gray-levels.

4.2.3 Calculated Values

Before calculating the required parameters, the noise floor is implemented. This means that all pixels having an intensity less than or equal to the noise floor are set to an intensity of zero.

4.2.3.1 Peak

The Peak is the pixel location (x,y) of the DALSA camera image found to have the highest intensity. If there is more than one pixel with the high intensity value, the first one found is displayed. Searching starts at the upper left hand corner and continues across the columns, left-to-right, in a raster-scan manner down to the bottom right.

4.2.3.2 Centroid

The centroid is calculated as follows:

$$\begin{aligned} mass &= \sum I(x,y), \\ X' &= \sum (x * I(x,y)), \\ Y' &= \sum (y * I(x,y)), \\ C_x &= X' / mass, \\ C_y &= Y' / mass, \\ C &= I(C_x, C_y) \end{aligned}$$

where *mass* is the sum of all the pixel values $I(x,y)$, X' & Y' are the horizontal and vertical centers of gravity, and the centroid intensity, C , is the pixel value at the coordinates (C_x, C_y) .

4.2.3.3 Fixed Location

The Fixed location coordinates are determined by the setting in Phase Generation Options (see section 4.2.5.1). The Intensity is the pixel value of the DALSA image found at the fixed location coordinates.

4.2.3.4 1st Moment

The first moment is calculated as follows:

$$m = \frac{\sum (x-X') (y-Y') I(x,y)}{mass^2}$$

4.2.3.5 Strehl Ratio

The Strehl ratio is the ratio of the energy in the peak, to the total energy in the image. The peak energy is found by summing the intensity at the peak pixel and the intensities within a Strehl radius (defined below) away from the peak power point.

$$S = \frac{\sum I(x,y)}{mass}$$

4.2.3.6 Strehl Radius

The Strehl radius only affects the value of the Strehl ratio. Valid values range from 1 to 256.

4.2.3.7 Noise Floor

The noise floor is used to negate the effects of camera noise. All pixel values below the noise floor value are set to zero before any calculations (for the centroid, 1st moment, Strehl ratio, etc.) are performed. Valid values for noise floor range from 0 to 255.

4.2.3.8 Normalize

If this check box is selected, then all of the image values are divided by the intensity of the peak power pixel, before calculations are performed on the 1st moment and Strehl ratio. Normalization will also affect the DALSA camera Image display.

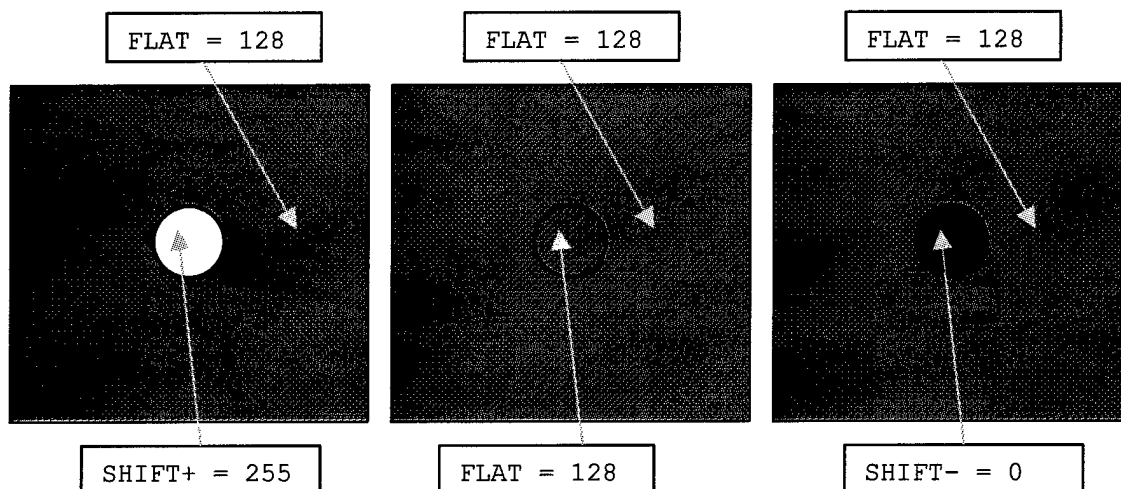


Figure 14. Three phase shifting options generated by *BNSWaveSense*.

4.2.4 Phase States

As seen in Figure 13, the software can modulate the SLM through three possible states, the "SHIFT+" state, the "FLAT" State, and the "SHIFT-" State. Check boxes are provided to the left of the states to enable or disable their use. If a state is not checked, it is simply skipped by the software. The values to the right of the states determine the pixel value, or voltage used during that state. These values are only used if the Phase Generation Option is selected to be the circle or the thresholding option. For example, Figure 14 shows the three SLM states generated when all three Phase States are enabled and "SHIFT+" = 255, "FLAT" = 128 and "SHIFT-" = 0.

4.2.5 Phase Image Generation Options

There are a variety of options to define the modulation characteristics of the SLM.

4.2.5.1 Circle Option

This option draws a circle of fixed size on the SLM. The position of the center of the circle is determined by the user selection, as either the centroid (marked in blue), the peak (marked in red) or a fixed location (marked in green). The radius of the circle can be adjusted from 0 to 256. Hooks are in the code to accept a calculated radius, dependent on the camera image, but no algorithm has been implemented at this time.

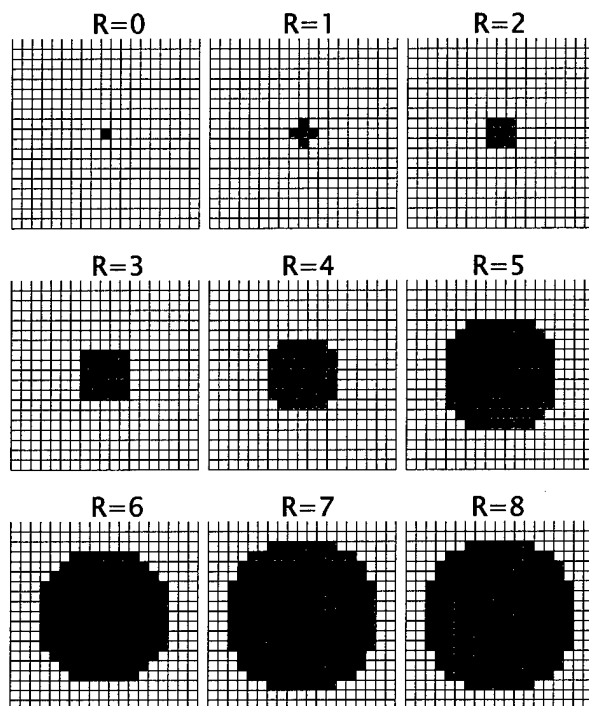


Figure 15. The circle pattern generated depends on its radius.

Figure 15 shows the pixels pattern generated for circles of various sizes. The circle is defined by the region:

$$d_x^2 + d_y^2 < r^2$$

where d_x is the distance from the center pixel on the x-axis, d_y is the distance from the center pixel on the y-axis, and r is the desired radius.

4.2.5.2 SLM=DALSA Option

When the SLM=DALSA option is selected, the image captured by the DALSA camera is fed directly to the SLM. Gray-levels of intensity (0-255) are simply converted to direct pixel voltages(0-255).

4.2.5.3 LUT File

The look-up table (LUT) function is not currently implemented. The idea of the LUT function is that when the SLM=DALSA option or the Alignment Mode Option are

selected, the LUT converts image values (0-255) to linear values of phase (0-128) calibrated to the SLM.

4.2.5.4 Threshold Option

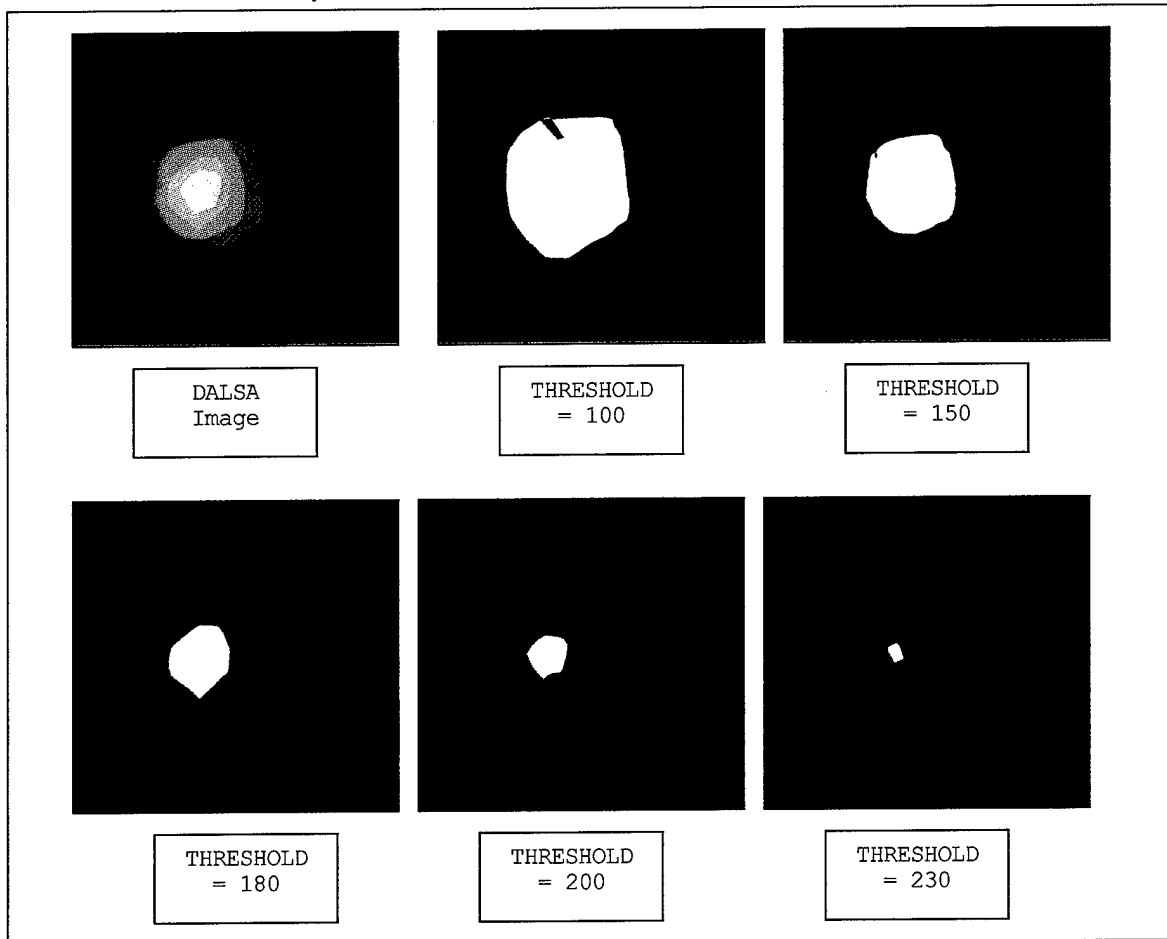


Figure 16. Implementation of the thresholding option.

The threshold option is used to modulate regions of the SLM that correspond to pixels above the specified threshold in the DALSA image. Figure 16 demonstrates this principle. If the image on the upper left were captured by the DALSA camera, the size of the modulation region would decrease as the threshold value is increased.

4.2.5.5 Alignment Mode Option

The alignment mode is used when first setting up the system. Under this option, the user may select a BMP image file from the hard-disk of the computer and have it display on the SLM. A crosshair pattern, as well as a set of vertical and horizontal stripes are provided with the system in the directory *C:\Program Files\Microsoft Visual Studio\MyProjects\BNSWaveSense\Images*.

4.3 Wave-front Sensor Speed

The goal of the Phase II system will be to reach 200 Hz operation. Therefore, it is important to measure the total system speed to determine if a faster approach will be required in Phase II.

The *BNSWaveSense* software was first written utilizing the library and device driver provided by National Instrument to access the PCI-DIO-96 data I/O board. Although the library provides adequate functionality to control the board, it does not provide it at a reasonable speed. It seems that between every write to an 8-bit I/O port, the device driver raises an interrupt and waits for the interrupt to be acknowledged before proceeding. This is very unfortunate, since the Data I/O board supports 96 output lines, 64 of which are used to stream data to the SLM driver board. The device driver only supports 8-bit writes, not a more useful 32-bit write. This means that in order to write an entire image to the SLM, we are required to perform 128K I/O port write instructions, with significant delays between writes. The system timing that has resulted is :

Task	Time Required
Grab Image from Camera	0.026 s
Display & Process Camera Image	0.422 s
Display SLM "SHIFT+" image	0.096 s
Download New Image to SLM	5.600 s
Display SLM "SHIFT-" image	0.096 s
Download New Image to SLM	5.600 s
Total	11.84 s

Table 1. Speed measurements of *BNSWaveSense* with the NI device driver.

This timing is obviously unacceptable. To solve this problem, we undertook the task of writing our own Window NT device driver for the PCI-DIO-96 board. The resulting speed improvement was:

Task	Time Required
Grab Image from Camera	0.028 s
Display & Process Camera Image	0.158 s
Display SLM "SHIFT+" image	0.080 s
Download New Image to SLM	0.216 s
Display SLM "SHIFT-" image	0.080 s
Download New Image to SLM	0.216 s
Total	0.778 s

Table 2. Speed measurements of *BNSWaveSense* with the BNS device driver.

Although an impressive improvement, the resulting speed is still less than 2 Hz and will not be acceptable in the final system.

It is likely that an appropriate electronic driver scheme can be found in Phase II to support 200 Hz operation. Of equal concern, however, is the response speed of the current 512x512 backplane and LC modulator. To determine this, BNS performed a simple experiment using our new 512x512 SLM driver board and a nematic LC-SLM with 2π of modulation depth at 800 nm. Two images, an all black image and an all white image, were placed in the driver board memory. A sequence that toggled between the two images was initiated and the output detected with a photodetector. Figure 17 shows the results of this test, with a measured relaxation time of 75 ms and an activation time of 25 ms.

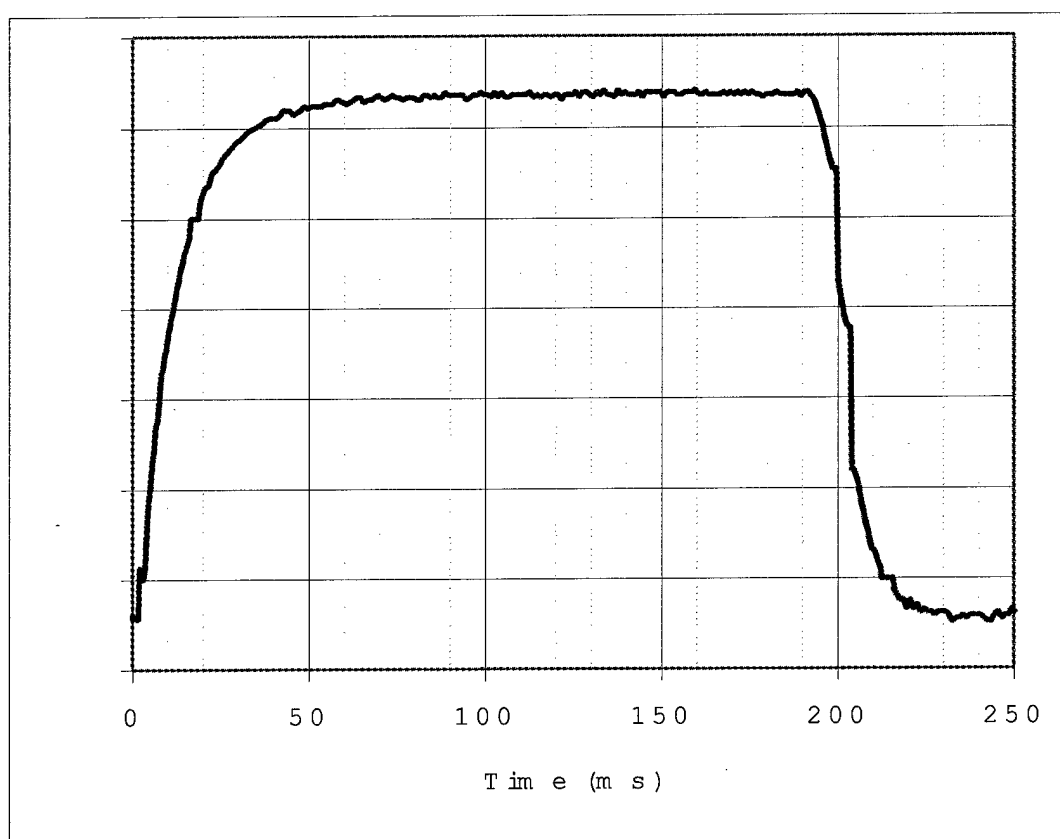


Figure 17. Speed of a nematic 512x512 (15 μm pitch) SLM, 2π @ 800.

4.4 Subtractive Imager Test Results

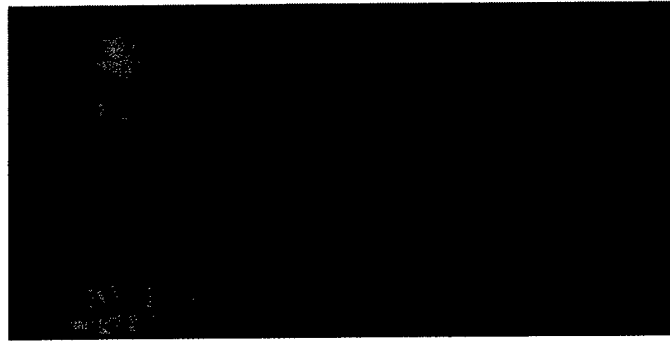


Figure 18. Sampled Intensity and difference Images from the subtractive imager.

Real life imagery from the TDI is shown in Figure 18. One of the two intensity images is shown on the right side, while the absolute difference is shown on the left side. In the difference image, the stationary background is zero, while the contour of the moving subject is visible. The measured fixed pattern noise in both intensity images is 0.8% of the saturation level.

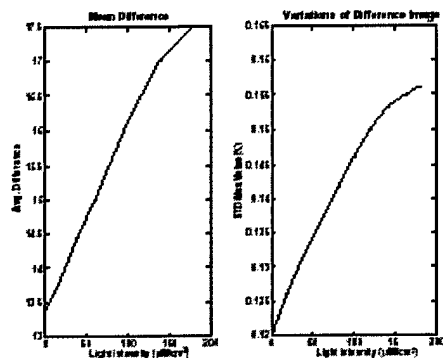


Figure 19. The mean and variation of the difference while in pipeline mode.

Figure 19 demonstrates the weak leakage dependency at the holding nodes on light intensity. The average difference and variations between the two outputs from all pixels in the entire image is measured as the illumination is increased. The entire image is measured as the illumination is increased. The average difference between the two images varies between 13.5 in weak light intensity to 17.5 in bright intensity, while the Intensity images vary of the whole 12-bit range. The variations also increase minimally with increasing light intensity, as seen in the right side of Figure 19. The pipeline architecture minimizes the variations in the difference computation. This permits for greater than 8-bit accuracy in the difference computation.

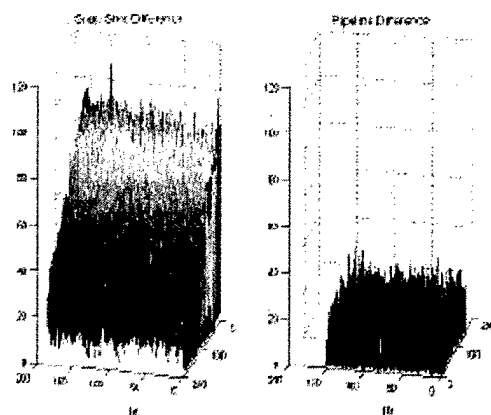


Figure 20. Comparison of snap shot (left) and pipelined (right) mode of operation at 150 mW light intensity.

The TDI can be programmed to operate in two different modes, as discussed previously. The first mode is snapshot mode, where two consecutive snap shots are obtained and the difference computed afterwards. In the operational mode, the leakage currents strongly influence the accuracy of the computed difference. As the difference is computed, the first pixel evaluated will have the least holding time and minimum leakage. As the image is evaluated, each additional pixel will have additional leakage time. The last pixel evaluated in the image will have the longest time delay. The leakage currents in this pixel will greatly affect the accuracy of the evaluated difference. The accuracy of this difference across the imager is demonstrated in Figure 20(a). The slope is evident in both the X and Y directions, as the image is scanned and the difference is evaluated.

The second mode of operation takes advantage of the pipeline architecture. Since all pixels will have the same holding time when operating in this mode, the variation due to leakage currents of the difference is minimized. The result of this minimization across the imager can be seen from Figure 20(b). The mean difference in this case is 16.5 with 0.14% variations of the maximum value. The advantage of the pipeline architecture over the snapshot operational mode is evident from the results presented in Figure 20.

Technology	0.5 μm Nwell CMOS
No. Transistors	120K
Array Size	189 x 182
Pixel Size	25 μm x 25 μm
Chip Size	5mm x 5mm
FPN	0.8% of sat. level
Fill Factor	30%
Dynamic Range	1 – 200 $\mu\text{W}/\text{cm}^2$
Frame Rate	30fps – 200fps
Saturation level	1.3V
Difference accuracy	> 8 bits
Power Consumption	30mW
Vdd = 5V@ 200 $\mu\text{W}/\text{cm}^2$	

Table 3. Subtractive Imager Chip characteristics

Table 3 shows the general characteristics of the chip. The total power consumption of 30 mW at 50 fps, makes this imager attractive for many applications. The 8-bit precision difference between two consecutive images, together with low fix pattern noise of 0.8% of saturation level is great advantage of this new architecture.

5 Conclusions and Recommendations

After reviewing the Phase II results, it is obvious that two elements of the wave-front sensing system will need to be improved; first the SLM modulation speed is too slow, and the SLM is not flat enough. The speed required is not completely known at this time, but we estimate that it may need to be about 200Hz.

5.1 Speed Improvements

There are a number of ways to improve the speed of wave-front sensing system that will need to be pursued in Phase II. There are two issues that determine the speed of the system, the electronic throughput, and LC-SLM response time.

5.1.1 Electronic Speed Improvements

The speed at which one can transfer the calculated SLM image from computer memory into the SLM driver board memory is an important consideration, and is currently the dominating speed bottleneck. The Phase I hardware is a very rudimentary prototype, with storage for only one image frame. In the Fall of 2001, BNS began shipping a new 512x512 driver board. This board supports the PCI bus, has 1024 frames of image memory on board, and can synchronize with a laser and/or camera. This board can be used as a basis to improve the electronic throughput in a number of ways.

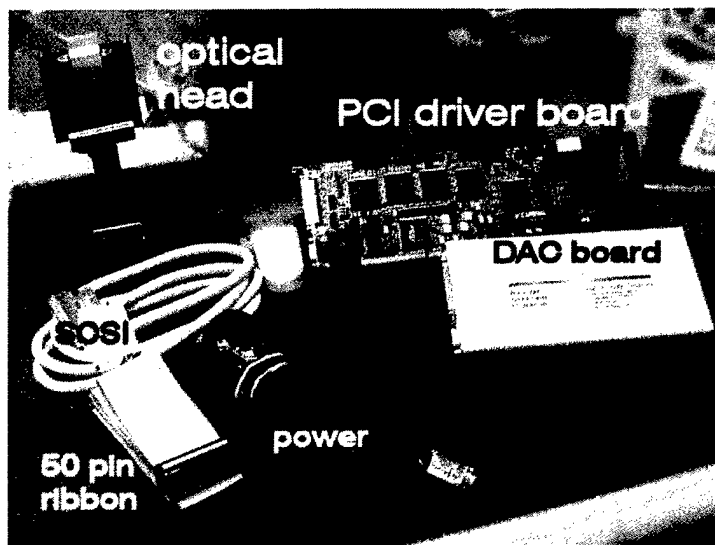


Figure 21. The new 512x512 driver board system.

5.1.1.1 Use the PCI Bus

The new 512x512 board utilizes a PCI bus interface. The PCI bus is specified to support an image download rate of 250 Hz when in burst mode, although the actual speed achieved is dependent on the machine and the number of other devices on the PCI bus. The current software device driver was based on code provided by the PCI chipset manufacturer, and is heavy with error-checking and overhead. To test the speed of this driver, we downloaded and displayed an all-white image, then an all-black image and measured the pixel voltage at the SLM. A maximum image load rate of 7.5 Hz was measured. By rewriting the device driver, we may be able to significantly increase the electronic data throughput.

5.1.1.2 Pre-Store all Images

The new 512x512 driver board has on-board memory for 1024 images. This would support 5 sizes of circles at 100 locations, for both the positive shift and negative shift images. The advantage of this scheme is that all the SLM images could be pre-calculated and pre-stored on-board, and then randomly accessed for loading to the SLM by a simple I/O address port write. This would increase the maximum electronic throughput to 1520 Hz, well above the rate of the LC material.

5.1.1.3 Direct feed through an External Port

The new 512x512 driver board has a 32-bit parallel port with direct feed into the driver board on-board memory. This port can load with a 100 MHz clock, allowing a new 512x512 image to be written in 655 μ s or 1525 Hz.

5.1.1.4 Calculated Processing on SLM driver board.

It is also possible, with some effort, to have the SLM driver board create the SLM modulation image. The external port of the SLM driver board is a programmable Xilinx FPGA. In this scenario, the control software would send the X and Y coordinates of the modulating circle, its size, and pixel value. The Xilinx chip would then generate the appropriate image and download it to the SLM. The speed of this process would be the same as the direct feed speed of 1525 Hz.

5.1.2 SLM Speed Improvements

Once the appropriate electronic voltages have reached the SLM, the response time of the LC modulator must be considered. The response of the LC material is, in general, dependent on the pixel/cover glass voltages, as well as the thickness and type of LC material. LC switching speeds are also strongly dependent on temperature, and heating the device may be considered if the performance gains justify the effort.

5.1.2.1 Use High Voltage VLSI Backplanes

Under an Air Force program, BNS is developing a new 256x256 backplane. The pixel pitch on this device will be 24 μ m. The AMI Semiconductor foundry in Pocatello, Idaho is

processing this device. The AMI foundry supports a high-voltage 0.5 μm process. Designers can use AMI Semiconductor's cells or transistors to create drivers with greater than 20-volt capability within the constraints of a cost-effective CMOS process.

Preliminary design simulations predict a maximum pixel voltage of 12V. This design includes a third "shiny metal" layer resulting in a 22.8 μm square pixel mirror. The fill factor is 90%. The die size will be approximately 10.4mm x 10.1 mm.

The first die are due back from the foundry in mid-Feb 2002. This system will use the same basic PCI driver board as the 512x512 system, but will include a modified external DAC board to drive the high voltages required by this chip.

5.1.2.2 Implement Cover Glass Flipping

Cover glass flipping is a strategy BNS has used in the past to double the effective field presented to the LC material, therefore increasing the switching speed. Figure 22 shows the current drive scheme. The cover glass is held at 2.5 V (red trace, pixel value = 127), and the pixels toggle at 2 kHz between their programmed value A ($A=63$ on blue trace or $A=21$ on green trace) and their inverse value $A'=(255-A)$. The field across the LC material at any given moment is the difference between the cover glass voltage and the pixel voltage. Therefore, using the current drive scheme, the maximum electric field is 2.5 V. There is also only 127 distinct modulation levels available, since a programmed level of A gives the identical electrical field strength as a programmed level at A' .

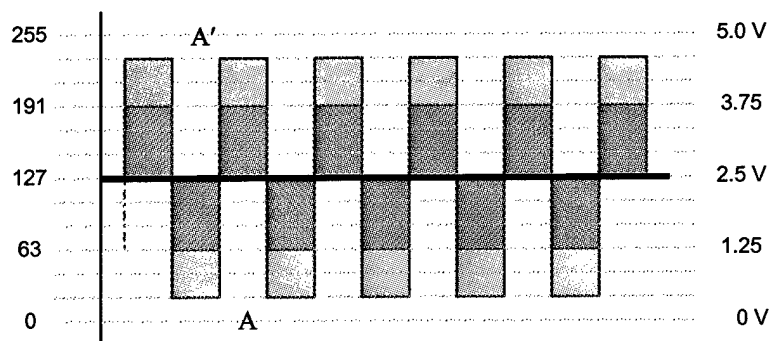


Figure 22. The current drive scheme.

The cover glass flipping strategy involves an active instead of a passive cover glass voltage, as shown in Figure 23. The cover glass (red) is synchronized to the opposite phase of the pixel voltage signal (e.g., blue or green). This scheme has two advantages, first, the maximum electric field across the LC layer has been doubled to 5.0 V, and second, a full 8-bits of modulation voltages are available.

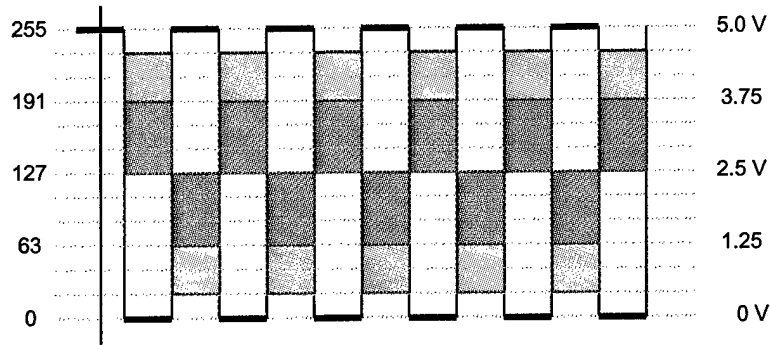


Figure 23. Cover glass flipping drive scheme.

The disadvantage of this scheme has to do with the addressing of the SLM pixel voltages. The SLM pixel voltages are refreshed in a raster scan manner, starting at the upper left corner, and finishing in the bottom right corner. When the cover glass voltage switches at the beginning of the SLM refresh, some pixels of the SLM will still have their old values. This field may be quite large, and it can take a fair amount of time for the image to settle at the new values.

5.1.2.3 Dual-Frequency LC Materials

Dual-frequency liquid crystal materials have a dielectric anisotropy that changes direction at a relatively low frequency. Because the material is driven on and off, it has much faster response than standard nematic materials. There are two dielectric constants for a LC material. The dielectric constant that applies when the long-axes of the molecules are parallel to the cell's surface is ϵ -perpendicular, since the E-field is directed perpendicular to the long axis of the molecule. Therefore, ϵ -parallel applies when the long axis of the molecule is perpendicular to the cell's electrodes. At low frequencies, ϵ -parallel is larger than ϵ -perpendicular causing the long axis to rotate into the field to increase the permittivity of the cell, minimizing the energy state of the molecules. As the frequency of the E-field increases, the difference between the two dielectric constants decreases and then changes sign with ϵ -perpendicular becoming larger than ϵ -parallel. After cross over, the intensity of the field is reduced by the long axis being perpendicular to the field, causing it to rotate away from the electrodes. All LC materials exhibit this type of behavior. However, the frequency and temperature where the cross over occurs is material dependent.

As part of an Air Force program, two dual-frequency materials were tested. The two dual frequency materials that we tested were NLC-999 and NLC-1001. Both of these materials were obtained from Igor Kompanets at the P.N. Lebedev Physical Institute in Moscow. To test the response time of these materials, we built a circuit that would allow the drive signal to be quickly switched between two different frequencies (from ~2 KHz to ~40 KHz). We found that one of the materials (NLC-999) produced considerable scatter and did not align well. It also seemed to be unstable. However, the other material (NLC-1001) performed as expected. At room temperature using the NLC-

1001, we were able to achieve a 275 μ s fall time (low frequency activation) and a 575 μ s rise time (high frequency activation). These values were achieved using a ± 20 volt drive signal. Figure 24 shows an oscilloscope trace demonstrating this performance. On Channel 1, the detector signal is displayed and Channel 2 shows the corresponding drive signal to the cell. Unfortunately, the two traces overlap making Channel 1 difficult to see, but the important information is the response time of the modulator, which corresponds to the rise and fall of the detector's signal. For the rise and fall times shown in the upper right hand corner of the plot, these values refer to a 10% to 90% transition of the detected light signal. The low-to-high or high-to-low transition of the light signal represents a π phase change, since the cell's optic axis is oriented at 45° to the input polarization and the cell is between crossed polarizers. Since the phase shift doubles for a reflective device, the rise and fall times of the transmissive cell actually represent 2π phase shifts for a VLSI-SLM.

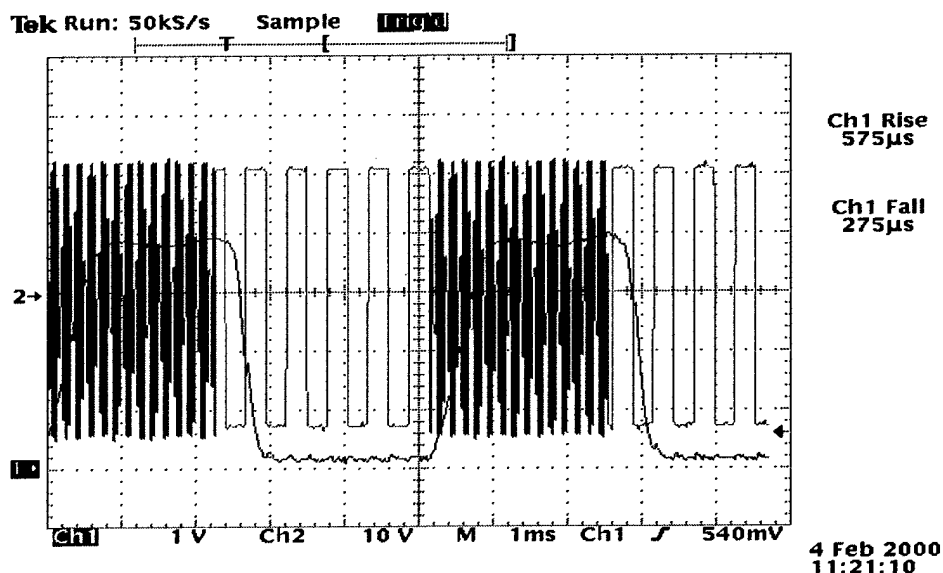


Figure 24. Oscilloscope outputs showing the drive signal and the corresponding optical response of a dual-frequency LC modulator. The on-to-off transition represents a π phase change for the transmissive cell, which is a 2π phase change in reflection.

Also, we characterized the NLC-1001 dual frequency material over temperature, voltage and frequency. The plot in Figure 24 shows the effect of temperature on the dual-frequency response of the modulator where fall and rise times were generated using ± 15 -volt 2 KHz and 40 KHz drive signals. The rise time (generated using the 40 KHz signal) is strongly affected by temperature. Below room temperature, the rise time has a local minimum and quickly rises as the temperature rises. Fortunately, this trend only lasts for 10 degrees and then the rise time quickly falls as the temperature approaches 40° C. At 40° C, the modulator's response (rise and fall) is impressive (< 300 microseconds combined) and appears to be stable.

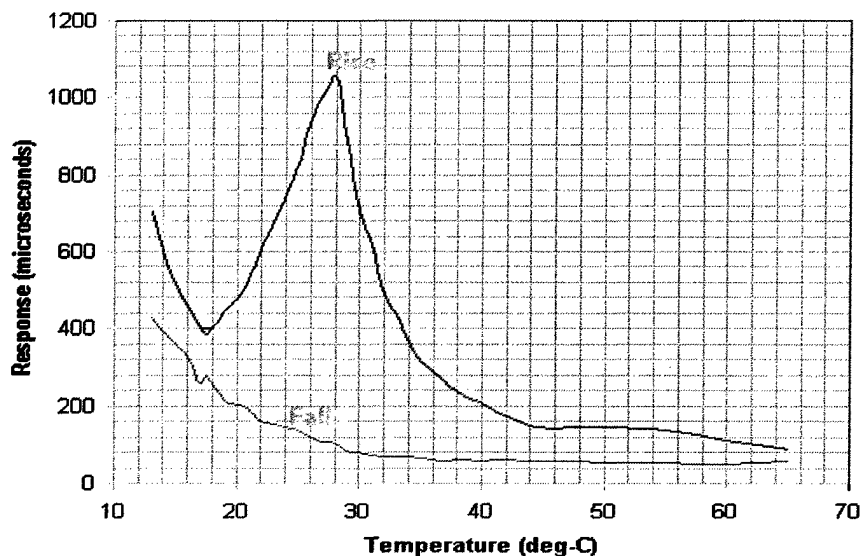


Figure 25. Plot of off-to-on (rise time due to 40 KHz activation) and on-to-off (fall time due to 2 KHz activation) transitions over temperature. Fall and rise transitions represent a π phase change at 633 nm for the transmissive modulator. A reflective device doubles this phase shift.

Under the Air Force program, we will be investigating the use of dual-frequency material with the new HV 256x256 chip. To achieve the 40 kHz frequency modulation required, we will be modulating the cover glass rapidly. Results should be available late this summer.

5.2 SLM Flatness Improvements

There have been two versions of the 512x512 SLM produced at BNS. The original device was based on a 5-volt, 1.2 micron VLSI process. The fill factor of this device was 60%. However, due to the relative ratio of the foundry process size and the pixel pitch, much of the pixel pad had a varying surface, due to the underlying electronic structures. These underlying structures, combined with the conformal nature of each processing layer, resulted in a poor optical throughput, with most of the light diffracting into the higher orders, and a low "flat fill" factor of 20%.



Figure 26. The original 512x512 SLM backplane as seen through a microscope.

A microscope image of some of the pixels on the original 512x512 SLM is shown in Figure 26. The area of one pixel is highlighted by the green rectangle. All of the structure that can be seen within one of these rectangles is due to a deformation from underlying layers of the silicon foundry process. As each layer is added, it conforms to the shape of the underlying layers, resulting in a highly diffractive device.

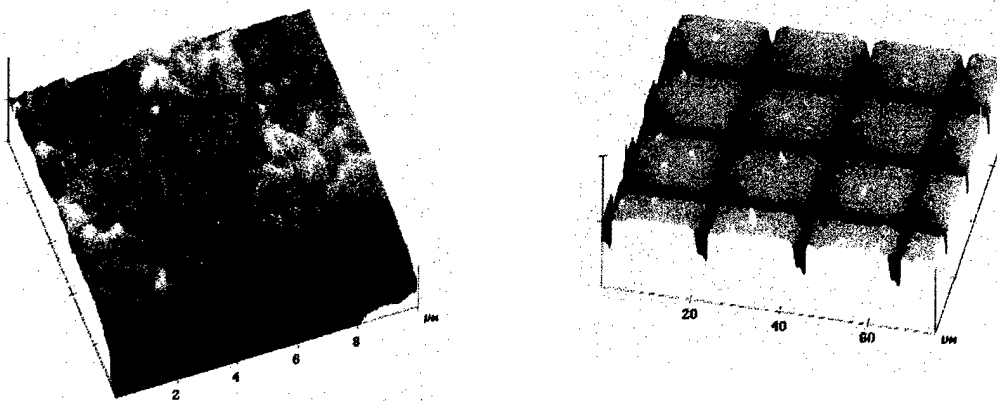


Figure 27. Atomic force microscope scans of an individual pixel and several pixels.

A second version of the 512x512 was created for a 3D-display manufacturer. The optical efficiency of the SLM backplane was a paramount importance to this company. To improve the optical quality of the existing pixels, the design was converted to a 0.5 micron silicon process. In recent years, as VLSI foundries have moved to smaller process sizes, they have begun performing CMP (Chemical Mechanical Polishing) between the metal layers. The flat surfaces allow the foundry to keep the entire mask in focus during processing. In addition to the CMP improvements, BNS added a third metal layer (M3) to the device design. The additional metal layer provides more options

for routing signals in the chip, plus adds light shielding for the underlying circuitry therefore preventing photo-conduction. The M3 metal layer increased the area fill factor from 60% (original design) to 80%. The M3 metal layer is also applied with a "shiny" metal technique. Typically, silicon foundries intentionally use low reflectivity metals to reduce the effects of stray light during photolithography steps. Figure 27 shows a typical M2 metal pixel with diffuse metal applied.

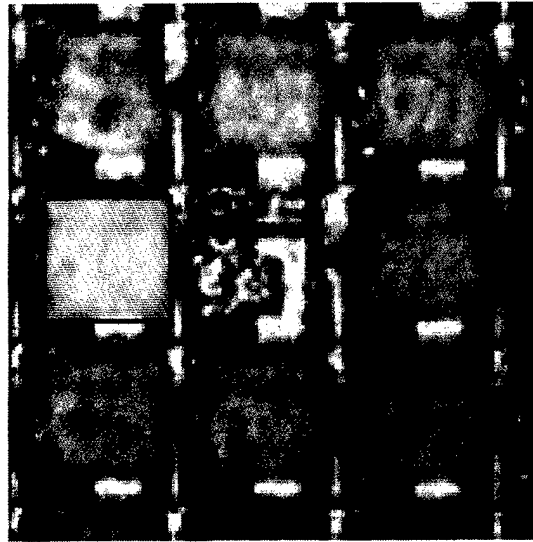


Figure 28. Microscope image of the new 512x512 SLM backplane. The green area outlines the size of a pixel. Note the bare test pixel in the center of the image, showing the underlying circuitry.

The "shiny" metal layer greatly improved the reflectivity of backplane, as seen in Figure 28. When a bare die of the original design was measured as a mirror, only 1% of the total power was diffracted into the zero order (DC). In contrast, the second design reflected 65.2% of the power in the zero order, a tremendous improvement in optical throughput.



Figure 29. CMP polishing improves local flatness, at the expense of global flatness.

Unfortunately, the CMP processing, which provided such tremendous improvements in the local flatness of the pixels, also produced a global irregularity in the die flatness. Figure 29 illustrates this fact. The CMP is performed on the entire wafer. Between the individual die on the wafer are deep "scribe lines" to facilitate the cutting apart of the die on the wafer. These scribe lines produce local hills and valleys that affect the height of the polished oxide layers. Subsequent layers conform and accentuate these irregularities. Figure 30 show the flatness of the device delivered to ARL. As one can see, there is almost 1.5 waves of curvature over the device.

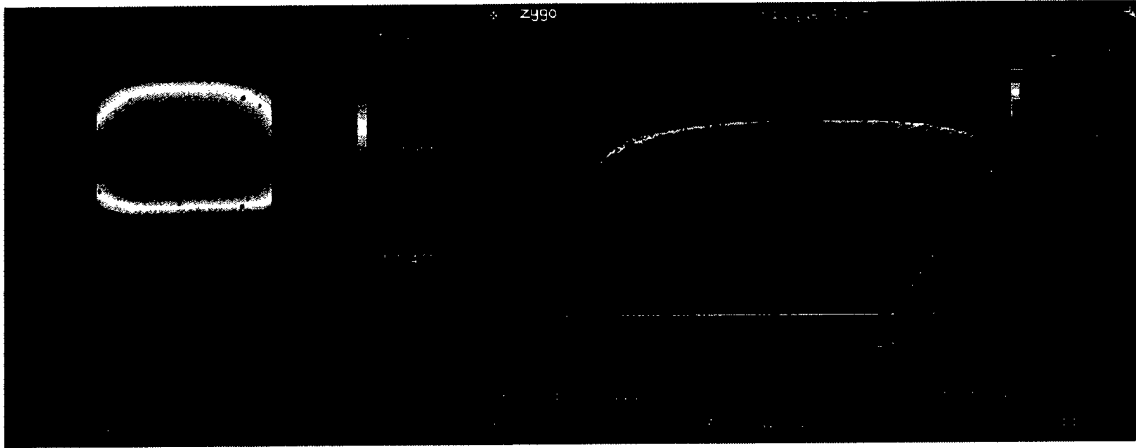


Figure 30. Zygo Interferometer scan of the 512x512 device, with a phase-shifted circle pattern applied³.

We believe the solution to this problem is to move the scribe lines as far away from the active area of the device as possible. Figure 31 shows the 512x512 device and Figure 32 shows the new 256x256 HV device. In the new device, dummy pixels have been added around the active area to increase the size of die, and move the scribe lines away from the active area, hopefully resulting in a flatter active area.

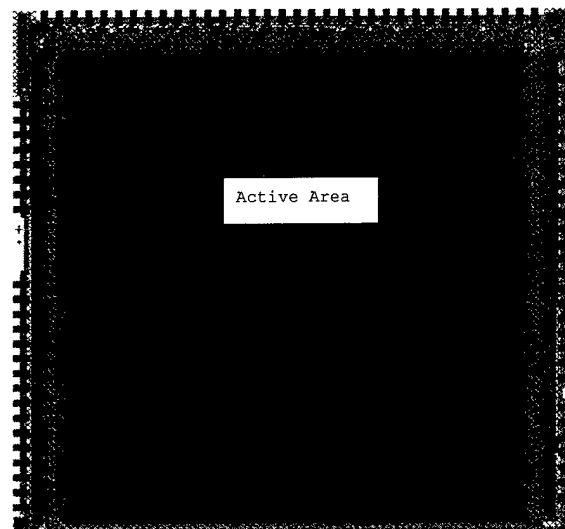


Figure 31. The 512x512 chip. The active area (dark purple) is 52% of the die size.

³ Data courtesy of Intelligent Optics Laboratory, Army Research Laboratory.

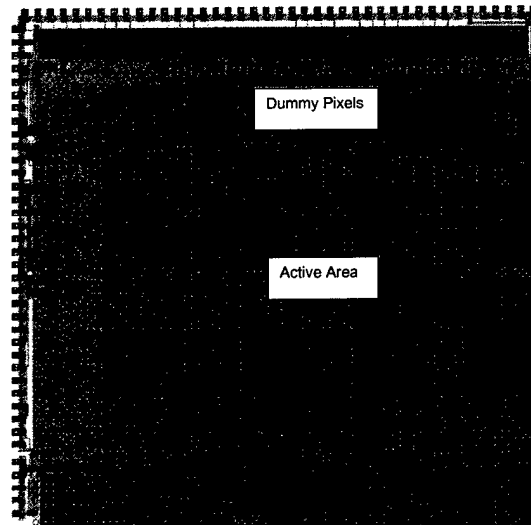


Figure 32. The HV 256x256 chip. The active area (green) is only 36 % of the die size, due to the additional dummy pixels (dark purple).

5.3 Summary of Phase I in Addressing the Technical Objectives

Revisiting the Phase I technical tasks (section 1.2) summarizes the conclusions from Phase I research.

- (1) A new subtractive imager chip was fabricated and evaluated by the team at Johns-Hopkins University. A new pipeline mode was implemented, decreasing the effects of leakage currents on the overall difference computation.
- (2) A prototype wavefront sensing system, including a computer, camera, frame-grabber, optics and LC_SLM was delivered to the Army Research Laboratory.
- (3) Under the direction of Dr. Justh, BNS developed custom software to process camera data and control the Fourier Filter SLM. This custom software offered the user maximum flexibility in operation, so that the LC-SLM device could be used in general-purpose optical experiments.
- (4) Researchers at the Army Research Laboratory evaluated the device and determined that the SLM device performed well in a phase-contrast setup. Speed and SLM device flatness continue to be an area of concern.

5.4 Recommendations for Further Development

Phase I work performed by BNS, Dr. Justh, JHU and ARL resulted in a prototype demonstration of a wave-front sensing system. The feasibility for successful use of LC-SLMs and Subtractive Imager chips in a complete wave-front sensing and control system was confirmed.

A second design and foundry run for the subtractive imager chip will need to be pursued in Phase II. The new design will further minimize leakage currents. In addition, a change in resolution and/or speed will be implemented.

System speed and LC-SLM device flatness are the primary issues raised by the Phase I research. It is the recommendation of BNS that improvements to software and electronics be pursued to improve the electronic throughput of the system. SLM modulator speed and flatness improvements are already being funded by the Air Force, and it is, as of yet, undetermined if additional Army funds will be required to meet the demands of the wave-front sensing and correcting system.

Phase II will primarily concentrate on development of the entire wavefront sensing and control feedback system. A dual-development will be proposed, where by a full system is shipped to ARL for system evaluation, while a second identical system is kept at BNS for development of further improvements to the system components.

In general, this complete Phase I feasibility study has produced no major stumbling blocks to discourage further development of the wave-front sensing and correction system. BNS recommends that the Army continue its commitment to this technology, which promises to be the next generation in adaptive optic technology.